

Improve gain flatness without sacrificing dynamic performance in high-IF ADCs

The proper selection of board components is essential to meet the demanding high-dynamic-performance and gain-flatness requirements for using analog-to-digital converters (ADCs) at high-IF input frequencies. High-IF ADCs are used in digital-communications systems: primary receive chain and predistortion circuits used in communications receivers and transmitters; high-speed instrumentation found in communications test systems; general broadband communications systems, satellites, and radar arrays. These ADCs are popular because they allow a system designer to reduce the number of down-conversion stages in the receiver signal chain and thereby reduce system costs. These devices generally yield excellent noise and distortion performance in the 2nd through 5th Nyquist regions.

The circuits discussed here convert a single-ended signal, which typically originates from a buffered demodulator circuit, to a differential signal to be fed to the high-IF ADC. These circuits use a wide-band transformer, termination resistors, and filter capacitors to accomplish this

task. Also discussed is the best termination scheme for the transformer to maintain a high-speed ADC's high dynamic range, while minimizing the effects of gain peaking and bandwidth reduction.

Single-ended-to-differential conversion with a 200MHz transformer

The MAX1449 was chosen for demonstration and analysis of two potential input configurations. **Figure 1** shows a typical, AC-coupled, single-ended-to-differential conversion design using a wide-band transformer, such as the T1-1T-KK81 (200MHz) from Mini-Circuits®, which has 50Ω primary-side termination and a 25Ω/22pF filter network. In this configuration, a single-ended signal from a 50Ω impedance source is converted to a differential signal through the transformer. Primary-side termination into 50Ω allows excellent matching between the signal source and the transformer. However, this also means that there is a mismatch between the primary and the secondary sides of the transformer. The primary side looks into a combined impedance of 25Ω, while the secondary side experiences a large impedance mismatch with the 20kΩ input resistance of the ADC shunted by 22pF. This impacts the frequency response of the input network, ultimately affecting the frequency response of the converter. The transformer's nominal leakage inductance can range from 25nH to 100nH. Combined with an input filter capacitor of 22pF, this creates a disturbing resonance frequency

$$f_0 = \frac{1}{2} \pi \sqrt{L_{\text{XFORMER}} \times C_{\text{IN}}}$$

occurring between 110MHz and 215MHz, which results in undesirable gain peaking in this frequency range.

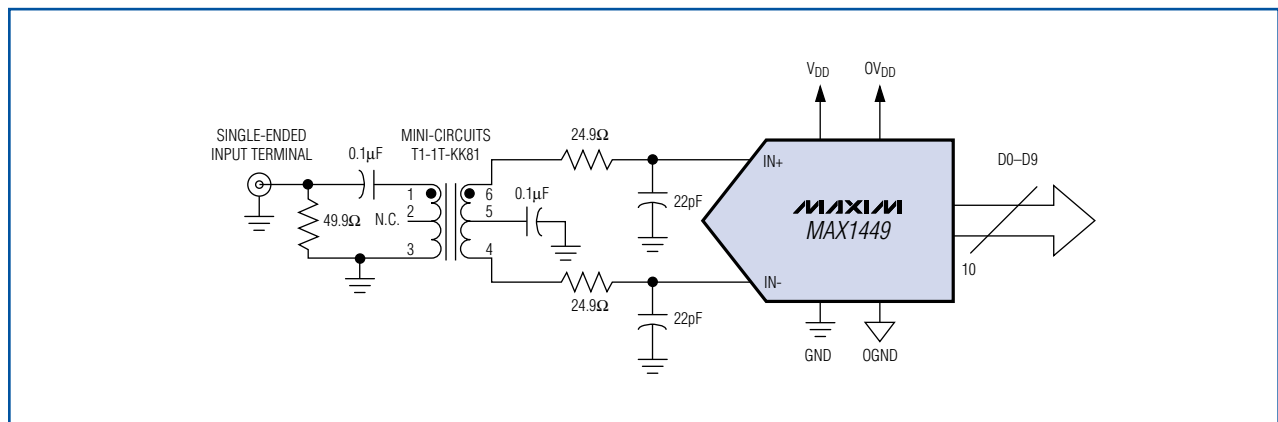


Figure 1. A single-ended signal from a 50Ω-impedance source is taken and converted to a differential signal through a 200MHz transformer.

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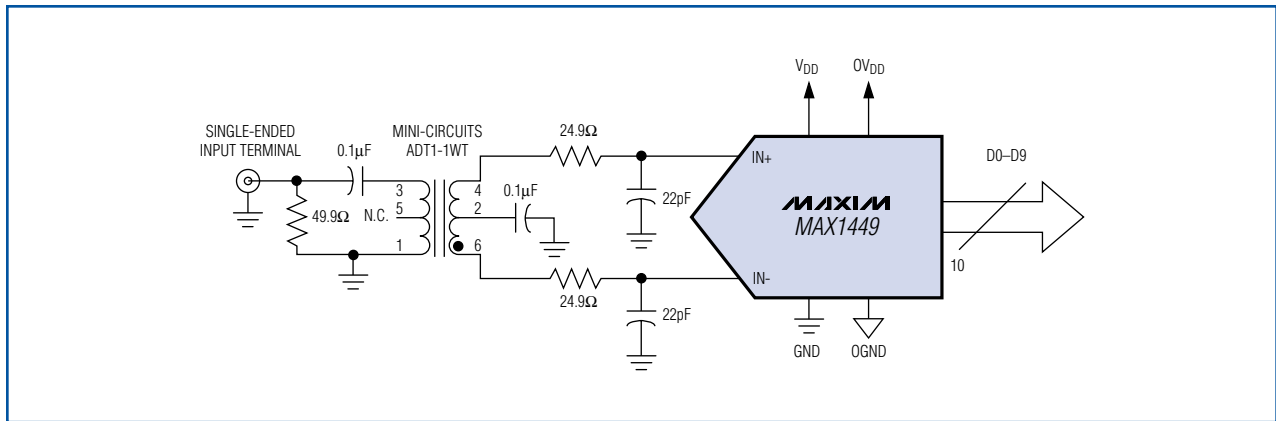


Figure 2. Similar to Figure 1, a single-ended signal is converted to a differential signal. However, this instance occurs through an 800MHz transformer, providing better performance.

Single-ended-to-differential conversion with an 800MHz transformer

Figure 2 depicts a similar AC-coupled configuration. However, this circuit was designed with a better performing wide-band transformer, such as Mini-Circuits' ADT1-1WT (800MHz), which includes a primary-side termination and a 25Ω/10pF filter network. Although, this transformer has an impedance of 75Ω, its lower leakage inductance yields a significantly better frequency response of -1dB up to 400MHz, compared to only 50MHz for the T1-1T-KK81.

Transformers—200MHz vs. 800MHz

Figure 3 shows the results for both termination schemes and selected filter network components and transformers. A significant improvement can be observed between the two graph plots. The input bandwidth plot for the T1-1T-KK81 transformer clearly shows a gain peaking of about 0.5dB between 90MHz and 110MHz, while the plot for the ADT1-1WT transformer remains flat within 0.1dB for frequencies up to 300MHz. The dynamic performance for this condition (ADT1-1WT transformer, 50Ω primary-side termination, and 10pF input filter capacitors at INP and INN) still yields an excellent SNR of 58.4dB for $f_{IN} = 50\text{MHz}$. Though Figure 3 only displays tested input frequencies of 80MHz and 260MHz (ADT1-1WT only), lab tests have proven that the gain remains flat within 0.1dB to input frequencies well beyond the 8th Nyquist region.

Matching the secondary-side impedance of the transformer can help to further enhance gain flatness. One way to do this is by using a secondary-side termination rather than a primary-side termination.

Particularly for high-IF applications, the location of the termination impedance is very important. Depending on the requirements for gain flatness and dynamic performance, an AC-coupled input signal can be terminated on either side of the transformer. Wide-band transformers are popular components that support a fast and easy way to convert a single-ended signal to a differential signal over a wide range of frequencies.

Primary-side termination

The MAX1124 (10-bit, 250Mps) was selected to demonstrate different termination schemes and their impact on gain bandwidth and dynamic performance of the ADC. Starting with a primary-side termination configuration (Figure 4a), a 50Ω impedance source signal is applied to

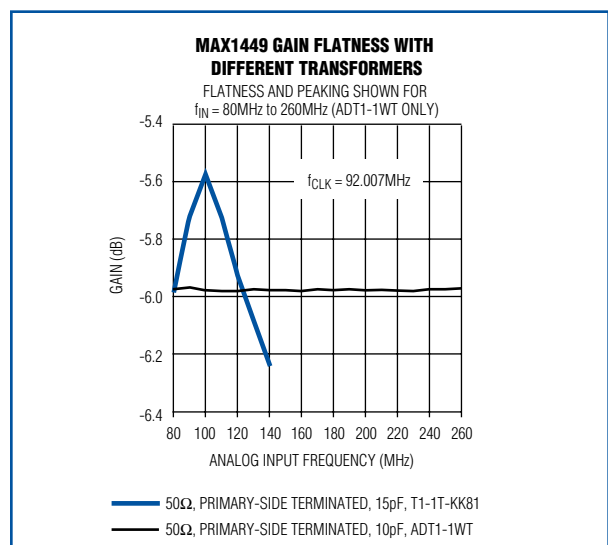


Figure 3. This graph illustrates the significant improvement in gain flatness obtained by using an 800MHz transformer vs. a 200MHz transformer.

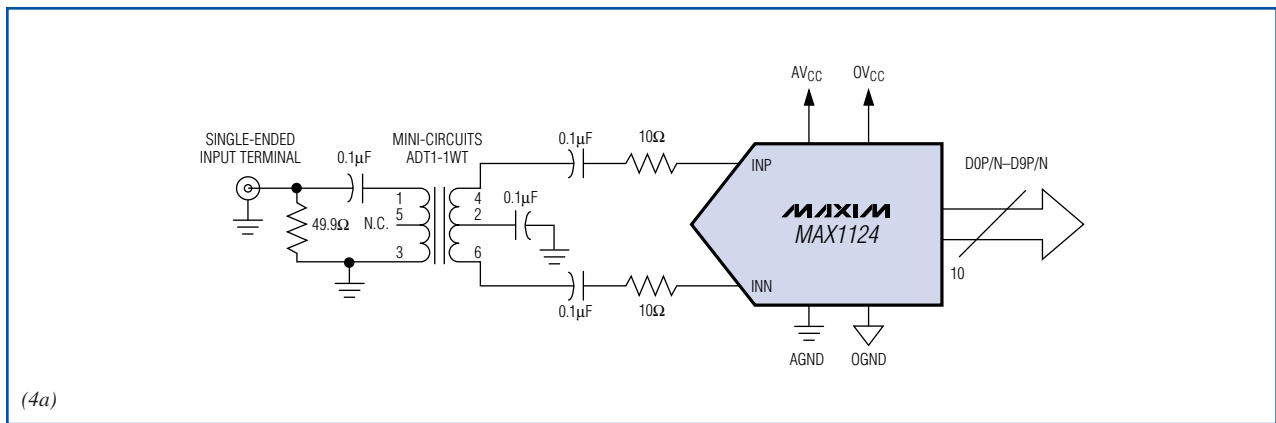
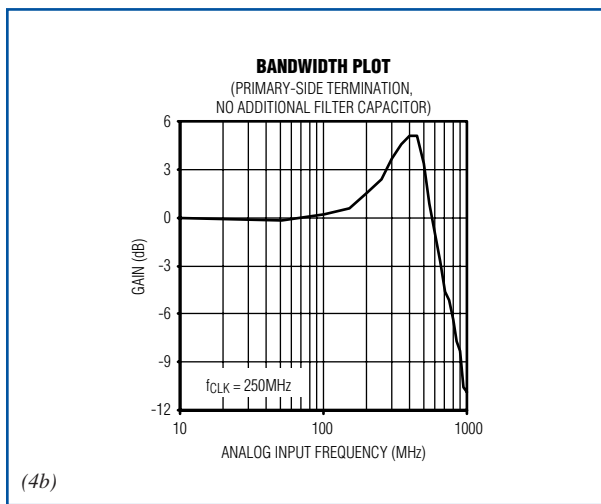


Figure 4. The well-balanced primary side of the transformer in this primary-side termination configuration (Figure 4a) is offset by an imbalance on the secondary side, producing maximum frequency peaking between 450MHz and 550MHz (Figure 4b).



the ADT1-1WT transformer's primary side. Its secondary side connects directly to the input filter network (10Ω isolation resistor and input impedance of the ADC) of the MAX1124 through 0.1μF AC-coupling capacitors. No additional input filter capacitors are installed on INP and INN. In this configuration, the primary side of the transformer is well balanced, though the secondary side looks straight into the nominal 4kΩ/3pF input impedance of the ADC. The imbalance on the secondary side, combined with the leakage inductance of the transformer, generates a resonant circuit, which produces maximum frequency peaking between 450MHz and 550MHz (Figure 4b).

Secondary-side termination

To eliminate frequency peaking almost completely while driving the input differentially, the primary-side termination is removed and the 50Ω source impedance signal is instead applied to the ADT1-1WT with secondary-side termination. In this case, secondary-side termination

means two 25Ω resistors are placed between the top/bottom and center taps of the transformer (Figure 5a). Followed by 0.1μF capacitors for AC-coupling purposes and an input filter network (15Ω series resistor and input impedance of the ADC), a well-balanced secondary-side signal is now applied to the converter. As with the configuration in Figure 4a, no additional input filter capacitors are installed on INP and INN. With this configuration, frequency peaking in the range of 450MHz to 550MHz can be completely eliminated. If required, more DC attenuation can be added by exchanging the 15Ω isolation resistors for 30Ω resistors. Although this approach makes the frequency response smoother, it causes a loss in frequency bandwidth (Figure 5b).

Conclusion

This article shows that not only the proper choice of passive components plays an important role in designing input networks for high-speed data converters, but the proper use of these components is significant as well. For instance, if gain flatness is an important factor in a system, care must be taken to avoid imbalances and resonances at the differential inputs of the converter to ensure that its true dynamic performance can be replicated. That both configurations do not use input filter capacitors might raise some concern about the impact of additional noise pickup at INP and INN. A brief analysis of this showed a degradation of the signal-to-noise ratio (SNR) between 0.2dB to 0.5dB. As long as wide bandwidth and stability over a wide range of frequencies (gain flatness) and a high dynamic performance are desired, most high-IF applications will accept this rather minor degradation in noise performance for a 10-bit data converter.

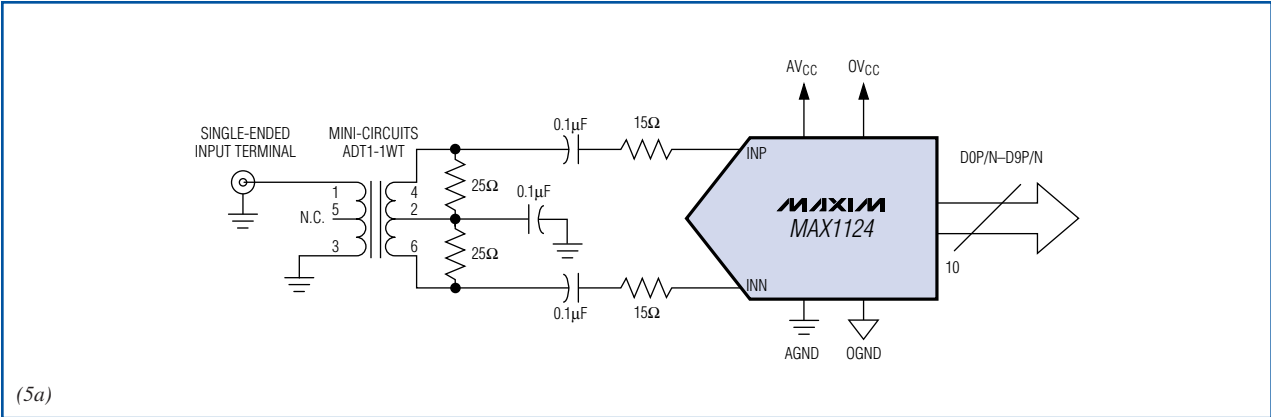


Figure 5. A well-balanced secondary-side signal is applied to the converter (Figure 5a), completely eliminating frequency peaking in the 450MHz to 550MHz range. DC attenuation can be increased, making frequency response smoother, but this will cause loss in frequency bandwidth (Figure 5b).

